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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,093	12/18/2001	Frank Matthews	5646-36	4976

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EXAMINER

DILLER, JESSE DAVID

ART UNIT	PAPER NUMBER
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2187

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/025,093	MATTHEWS ET AL.	
	Examiner	Art Unit	
	Jesse Diller	2187	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 16 December 2004.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) 10-12,21,22 and 35 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 4,8,13-20,23-34 and 36-38 is/are allowed.
- 6) ☒ Claim(s) 1-3 and 7 is/are rejected.
- 7) ☒ Claim(s) 5,6 and 9 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 March 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Amendment***

1. Examiner acknowledges the receipt of the amendment in response to the office action dated 12/3/2004, which amendment was received 12/16/2004. At this point, claims 10-12, 21-22, and 35 have been cancelled, and claims 4, 8, 13, 19, 23, 29, and 35 have been amended. Thus, claims 1-9, 13-20, 23-34, and 36-39 are pending in the application.

### ***Response to Amendment***

#### **Objections to the disclosure**

2. In response to amendment, the objections to the abstract and specification have been withdrawn.
3. The Examiner would like to thank the applicants for their clarification/explanation of Fig. 3; accordingly, the objection to Fig. 3 is withdrawn.

#### **Response to Arguments**

4. Applicant's arguments filed 12/16/2004 with respect to claim 1 have been fully considered but they are not persuasive.
5. On page 15 of said arguments, applicant contends that independent claim 1 is patentable over Ito, US Patent 5,321,652. Specifically, applicant contends that, in Fig. 2 of Ito,

*"Ito provides absolutely no disclosure or suggestion of any "overwriting" of any data within a pulsed sense amplifier, as recited by independent Claim 1. For example, the data (dr0-drn) in the read amplifier B (RAB) in FIG. 2 of Ito is not overwritten with any of the data (da0-dan) from the data buffer B. Instead, the data selector DSL merely selects data from one device or another device in response to a detection signal "am".*

6. The Examiner agrees with the example provided; however, the example is not consistent with what Ito teaches. Ito does not teach that data (dr0-drn) in the read amplifier B (RAB) is overwritten with any of the data (da0-dan) from the data buffer B. Ito teaches that data from either read amplifier B or data buffer A is selectively routed to data buffer B. Data in data selector DSL is the logical inverse of input data, and the data output from DSL on data lines db0-dbn is the same as the input data. It is plainly evident that before the assertion of match signal *am*, the DSL outputs (i.e. db0-dbn) hold the latched second data dr0-drn. Upon the assertion of the match signal *am*, the *latched second data from read amplifier B* (i.e., dr0-drn) which was previously held at the output (i.e., db0-dbn) is overwritten by the first data from data buffer A (i.e., da0-dan) which propagates through the DSL. As applicants recognize, the data selector DSL selects data from one device or another device in response to a detection signal "am". When the match signal is asserted or negated, the data within the DSL and the data at the output of the DSL *is replaced* by data from the other input and is lost.

7. Accordingly, the rejection under 35 USC 102(b) is deemed to be proper.

***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-3 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Ito, US Patent #5,321,652.

10. As for claim 1, Ito teaches:

- In an integrated circuit memory device (IC CHIP, Fig. 1) comprising a memory array (MARY, Fig. 6; Col. 3, lines 56-59) having first and second ports (MULTIPOINT MEMORY, Fig. 1; Fig. 6) that can each support asynchronous read and write access (Col. 1, lines 26-41; Col. 13, lines 5-8) and a pulsed sense amplifier (split multistage amplifier: RAB and DSL, Fig. 2) that receives data (dr0-drn, Fig. 2) from the second port (DB0-DBn, Fig. 6) a method of operating the memory device, comprising the steps of:
- writing first data (da0-dan, Fig. 6) from a data input buffer coupled to the first port (DBA, Fig. 6) to a write address in the memory array while simultaneously writing a copy of the first data to a bypass latch (CN1-6, Fig. 2) associated with the second port (Fig. 2 shows a copy of the first data da0-dan written to the input of the latched DSL);

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- reading second data from a read address in the memory array by activating the pulsed sense amplifier (DSL, Fig 2) to latch the second data (Col. 8, lines 33-38); and
- overwriting the latched second data with the copy of the first data from *said bypass latch* (see 35 USC 112 2<sup>nd</sup> rejection of claim 1 above; before the assertion of match signal *am*, Fig. 2, the DSL outputs *db0-dbn* hold the latched second data *dr0-drn*. Upon the assertion of the match signal *am*, the latched second data *dr0-drn* at the output *db0-dbn* is overwritten by the first data *da0-dan*)

11. As for claim 2, Ito additionally teaches:

- the second data is latched in response to a leading edge of a latch enable signal (see DSL, Fig. 2; the latch is enabled by the match signal *am*; the second data is latched on the falling edge of *am*); and wherein
- the latched second data is overwritten with the copy of the first data from the bypass latch in response to a trailing edge of the latch enable signal (the rising edge of signal *am* latches the first data to overwrite the second data).

12. As for claim 3, Ito additionally teaches:

- the method of Claim 1, wherein said writing step comprises
- overwriting old data at the write address with new data; and wherein
- the second data latched by the pulsed sense amplifier is the old data (Fig. 5 teaches that *when there is coincidence of the read/write addresses*, *dr0-drn* holds old data at first; later, *dr0-drn* hold the new data read from the memory

array. However, db0-dbn transitions to its final value before the transition of the read linesdr0-drn. As shown in Figure 2, on the falling edge of signal *am* until the rising edge, the data latched into the DSL is the data from the second port (DBA, Fig. 2). Therefore, before the final transition of the output lines db0-dbn to hold the first data, the sense amplifier had latched old data. Also see Col. 12, lines 24-30).

13. As for claim 7, Ito additionally teaches:

- comparing (AC, Fig. 2) the write address (aa0-aan) to the read address (ab0-abn); and generating a leading edge of a match signal if said comparing step indicates an equivalency (Col. 7, line 65 - Col. 8, line 6).

#### ***Allowable Subject Matter***

14. As per applicant's amendment dated 12/3/2004, Claims 4, 8, 13-20, 23-34, and 36-38 are allowed.

15. Claims 5-6, and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

16. The primary reason for allowance of claim 5-6 in the instant application is the combination with the inclusion in these claims that the leading edge of the latch enable signal is a falling edge. The prior art of record does not anticipate the above recited combination.

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17. The primary reason for allowance of claim 9 in the instant application is the combination with the inclusion in these claims of a distinction between the match signal and latch enable/loopback signals. The prior art of record neither anticipates nor renders obvious the above recited combination.

18. If the applicant should choose to rewrite the independent claims to include the limitations recited in either one of claims 4-6, 8-9, 13-20, 23-30, 31-34, and 36-38, the applicant is encouraged to amend the title of the invention such that it is descriptive of the invention as claimed as required by sec. 606.01 of the MPEP. Furthermore, the Summary of the Invention and the Abstract should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of sec. 1302.01 of the MPEP.

19. As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and § 707.07(a) of the M.P.E.P.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within



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TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

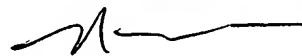
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse Diller whose telephone number is (571)272-4173. The examiner can normally be reached on 8:00AM-4:30PM, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571)272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
JD

**NASSER MOAZZA**  
**PRIMARY EXAMINER**

  
1, 15, 05